Remarks

Applicant greatly appreciates the Examiner's consideration of Applicant's argument filed February 5, 2003 and withdrawal of the rejection under §102(e). In the outstanding Office Action, the Examiner has rejected claims 1-41 under 35 U.S.C. §103(a) as being unpatentable over Lam, United States Patent Number 6,281,046, (hereinafter "Lam") in view of admitted prior art described on pages 2-4 of the specification.

Claims 1-41 were originally presented for Examination. Claims 1, 18 and 36 are amended by way of the present Response. Claims 1-41 are currently pending, of which, claims 1, 18 and 36 are in independent form. Favorable reconsideration of the present amendment as currently constituted is respectfully requested.

Rejection Under 35 U.S.C. §103(a)

Claims 1-41 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Lam in view of Applicant's disclosure on pages 2-4 of the Specification. The present invention, as defined by independent claim 1, is directed to a method for selecting components for a matched set. The method includes simultaneously testing at least two of the integrated circuit chips of the semiconductor wafer to determine inclusion in the matched set and selecting at least two of the chip assemblies corresponding to the at least two the integrated circuit chips for inclusion in the

matched set based upon the simultaneous testing. Existing methodologies employ data from individual testing in order to determine component compatibility. Applicant's method overcomes the limitations of the prior art by employing a wafer-interposer assembly in order to simultaneously test at least two of the integrated circuit chips of the semiconductor wafer to determine inclusion in the matched set prior to singulation. By simultaneously testing the components to determine inclusion in the matched set, Applicant's present invention avoids certain mismatches that are not identified until the entire chip collection is assembled and the components are tested together for the first time.

Applicant respectfully submits that the method for selecting components for a matched set as recited in claim 1 is neither disclosed nor suggested by Lab. Lam discloses a method for packaging a semiconductor die at the wafer level using one interposer sheet for the entire wafer. Lam describes his testing procedures as follows:

> At this point, electrical testing may be conducted on the wafer/interposer assembly 39 since the wafer assembly 39 contains finished dice arranged in a matrix format. This allows for parallel testing which can be conducted at the wafer level and can provide savings in testing time and cost. Then the wafer/interposer assembly 39 is diced, or singulated, such as along line 60, to form individual chip-size BGA packages 70, 72. A common technique for the singulation is to use a wafer saw with diamond or resinoid saw blades. With reference to FIG. 9, the finished BGA package 70 of the present invention has the same footprint as the individual silicon die, as no extra space is needed to accommodate

> wirebond leads or larger substrate bases. In this way, the integrated circuit package of the present invention provides the advantages of a smaller package size and the convenience of packaging at the wafer level. Column 5, lines 19-37.

Assuming *arguendo* that Lam discloses simultaneous testing of at least two integrated circuit chips of a semiconductor wafer, as stated by the Examiner, Lam does not disclose or suggest either simultaneously testing at least two of the integrated circuit chips of the semiconductor wafer to determine inclusion in the matched set prior to singulation or selecting at least two of the chip assemblies for inclusion in a matched set based upon the simultaneous testing. In particular, Lam describes the parallel testing as wafer level testing that provides a "savings in testing time and cost." Lam does not disclose performing simultaneous testing in order to determine inclusion in the matched set. Lam performs parallel testing in order to save time and cost by parallel testing all of the wafers while the wafers are in one location.

These deficiencies are not cured by the application of Applicant's Background of the Invention. Applicant respectfully submits that the method for selecting components for a matched set as recited in claim 1 is neither disclosed nor suggested by the combination of Lam and Applicant's Background of the Invention. In particular, the steps of simultaneously testing at least two of the integrated circuit chips of the semiconductor wafer to determine inclusion in the matched set prior to singulation and selecting at

least two of the chip assemblies corresponding to the at least two of the integrated circuit chips for inclusion in the matched set based upon the simultaneous testing are not found in the combination.

Applicant traverses the Examiner's characterization of the Background of the Invention. The Examiner has characterized Applicant's Background as expressly teaching the step of selecting at least two chip assemblies for inclusion in a matched set based upon simultaneous testing. To the contrary, Applicant's background discloses assembling singulated components which may be identical or dissimilar as a matched set following the testing of each component **individually**, not simultaneously prior to singulation which is the prior art problem the present invention is specifically designed to overcome. Specifically, the Applicant states the following in the Background of the Invention:

> One approach for improving system performance is through the use of matched sets. For example, several identical or dissimilar components that have been identified by the **individual testing phase** of component processing to have certain performance tracking characteristics may be assembled together as a matched set. The components of such a matched set are frequently attached to a single substrate in close proximity to one another. This strategy improves performance compared to conventional or non-optimized systems by reducing the overall space needed to accommodate the chips and by, among other things, shortening the distance between chips. Specifically, interconnect inductance and signal transmission delays are all reduced.
>
> One type of matched set includes a collection of identical components which have been identified to meet specific system performance requirements....Typically, each of the identical components has been extensively **tested individually** prior to

> inclusion in this type of system.... [M]ulti-dimensional arrays of data are then compared to each other to identify individual components that perform within acceptable limits relative to each other. Components that are found to exhibit similar behavior under the various input stimuli will constitute a matched set of identical devices. Conversely, components that are found to exhibit dissimilar behavior under the various input stimuli...will constitute a mismatch of components that will not be placed in a chip collection.
>
> It has been found, however, the certain mismatches are not identified when the components are tested individually. In fact, certain mismatches are not identified until the entire chip collection is assembled and the components are **tested together for the first time**. Emphasis added. Page 2, line 20 - Page 4, line 10.

During the course of discussing the individual testing of components, Applicant states the following: "each of the individual components has been extensively **tested individually prior** to inclusion in the system;" "certain mismatches are not identified when the components are **tested individually**;" and "certain mismatches are not identified until the entire chip collection is assembled and the components are **tested together for the first time**." Applicant's background neither discloses nor suggests selecting components based upon simultaneous testing of chips on a wafer prior to singulation. To the contrary, Applicant's Background of the Invention discusses the long felt need for improving the matched set component selection process and identifies the limitations of testing components individually. Applicant respectfully submits that the Examiner has inappropriately characterized Applicant's background as disclosing

the step of selecting at least two chip assemblies for inclusion in a matched set based upon the simultaneous testing of the integrated circuit chips of the semiconductor wafer. Accordingly, even if Lam and Applicant's Background of the Invention were combined as proposed by the Examiner, the method for selecting components for a matched set as recited in claim 1 would not be found in the combination. Accordingly, Applicant respectfully requests withdrawal of the outstanding §103(a) rejection and allowance of claim 1.

Claims 2-17 depend from independent claim 1 and introduce further limitations in combination therewith. Therefore, the allowance of claims 2-17 is respectfully requested.

The present invention, as defined by independent claim 18, is directed to a method for assembling a matched set. Similar to claim 1, claim 18 includes limitations directed to providing a semiconductor wafer having a plurality of integrated circuit chips, coupling the wafer to an interposer to form a wafer-interposer assembly, and simultaneously testing pairs of the integrated circuit chips of the wafer to determine inclusion in a matched set. Accordingly, for the reasons presented hereinabove, Applicant respectfully requests withdrawal of the outstanding §103(a) rejection and allowance of claim 18.

Claims 19-34 depend from independent claim 18 and introduce further limitations in combination therewith. Therefore, the allowance of claims 19-34 is respectfully requested.

The present invention, as defined by independent claim 35, is directed to a matched set assembled by the method as recited in claim 18. Accordingly, for the reasons presented hereinabove, Applicant respectfully requests withdrawal of the outstanding §103(a) rejection and allowance of claim 35.

The present invention, as defined by independent claim 36, is directed to a matched set of integrated circuit chips. Similar to claim 1, claim 36 includes limitations directed to simultaneously testing first and second chip assemblies that are a part of a wafer-interposer assembly to determine inclusion in a matched set. Accordingly, for the reasons presented hereinabove, Applicant respectfully requests withdrawal of the outstanding §103(a) rejection and allowance of claim 36.

Claims 37-41 depend from independent claim 36 and introduce further limitations in combination therewith. Therefore, the allowance of claims 37-41 is respectfully requested.

Conclusion

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding objections and rejections and allow claims 1-41 presented for reconsideration

herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested. The Examiner is requested to call the undersigned for any reason that would advance the instant application to issue.

Fee Statement

Applicant believes no additional fees are due for the filing of this Response. If any fees are due, or any overpayments have been made, however, please charge, or credit, our Deposit Account No. 03-1130.

The Examiner is requested to call the undersigned for any reason that would advance the instant application to issue.

Dated this 23rd day of April, 2003.

Respectfully submitted:

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